WHAT IS CLAIMED IS:

1. A thin film transistor comprising:

a current path pattern defining a current path, said current path pattern being made of semiconductor material and formed on a substrate;

a gate pattern crossing said current path pattern at least in first and second cross areas, said gate pattern defining a channel region of said current path pattern in an area superposed upon by said gate pattern; and

a gate insulating film disposed between said current path pattern and said gate pattern in the first and second cross areas,

wherein said current path pattern has an LDD structure on both sides of the channel region in the first cross area, the LDD structure including low concentration regions in contact with the channel region and high concentration regions in contact with the low concentration regions, and has an impurity concentration in areas in contact with the channel region in the second cross area higher than an impurity concentration of the low impurity concentration regions.

2. A liquid crystal display substrate comprising:

a plurality of gate bus lines extending in a row direction and formed on a substrate;

a plurality of drain bus lines extending in a column direction and formed on the substrate, said drain bus lines being electrically insulated from said gate bus lines in cross areas in which said gate bus lines cross with said drain bus lines;

pixel electrodes disposed in cross areas between said gate bus lines and said drain bus lines;

current path patterns corresponding to cross points between said gate

bus lines and said drain bus lines, said current path patterns being made of semiconductor material and crossing a corresponding gate bus line at least at two points, channel regions of said current path patterns being formed in areas superposed upon by said gate bus lines, a first end portion of each said current path pattern being electrically connected to a corresponding drain bus line, and a second end portion of each said current path pattern being electrically connected to a corresponding pixel electrode; and

gate insulating films disposed between said gate bus lines and said current path patterns in the cross area,

wherein each said current path pattern has an LDD structure on both sides of the channel region nearer to the first end portion, the LDD structure including low concentration regions in contact with the channel region and high concentration regions in contact with the low concentration regions, and has an impurity concentration in areas in contact with the channel region nearer to the second end portion higher than an impurity concentration of the low impurity concentration regions.

3. A method of manufacturing a semiconductor display substrate, comprising the steps of:

preparing a substrate on which an image display area and a peripheral circuit area are defined, the peripheral circuit area being disposed at a side of the image display area;

forming a plurality of first current path patterns distributed in a matrix shape on the substrate in the image display area and a second current path pattern in the peripheral circuit area, in such a manner that each of the first current path patterns includes a portion flowing current at least in a column direction and the

second current path pattern includes a portion flowing current at least in a row direction;

covering the first and second current path patterns with a gate insulating film;

forming a plurality of gate patterns on the gate insulating film in such a manner that the gate pattern crosses the column directionally flowing current portion of the first current path pattern in the image display area and crosses the row directionally flowing current portion of the second current path pattern in the peripheral circuit area;

implanting impurity ions into the first and second current path patterns by using the gate patterns as masks; and

irradiating an energy beam into the first and second current path patterns along an oblique direction relative to the substrate surface to activate doped impurities so that the energy beam is irradiated in the first current path patterns in a shaded state of one of both sides of the gate patterns and irradiated in the second current pattern on both sides of the gate pattern.

4. A liquid crystal display substrate comprising:

a substrate on which an image display area and a peripheral circuit area are defined, the peripheral circuit area being disposed at a side of the image display area;

a plurality of gate bus lines extending in a row direction and formed on the substrate in the image display area;

a plurality of drain bus lines extending in a column direction and formed on the substrate in the image display area, said drain bus lines being electrically insulated from said gate bus lines in cross areas in which said drain bus

lines cross with said gate bus lines;

pixel electrodes corresponding to cross areas in which said drain bus lines cross with said gate bus lines;

first thin film transistors corresponding to the cross areas in which said drain bus lines cross with said gate bus lines, each of said first thin film transistors connecting corresponding drain bus line and pixel electrode, each of said first thin film transistors including a channel region for flowing current in a first direction, first impurity doped region having a first impurity concentration, and second impurity doped region having a second impurity concentration higher than the first impurity concentration, said first impurity doped region and said second impurity doped region sandwiching said channel region, current flowing in the channel region being controlled by a corresponding gate bus line, and the first impurity doped region being electrically connected to a corresponding said drain bus line; and

a second thin film transistor formed on the substrate in the peripheral circuit area and including a channel region for flowing current in a second direction perpendicular to the first direction, and third impurity doped regions having a third impurity concentration and disposed on both sides of the channel region.

5. A liquid crystal display substrate according to claim 4, further comprising:

a third thin film transistor formed on the substrate in the peripheral circuit area and including a channel region for flowing current in the first direction, fourth impurity doped region having a fourth impurity concentration, and fifth impurity doped region having a fifth impurity concentration higher than the fourth impurity concentration, said fourth impurity doped region and fifth impurity doped region sandwiching said channel region;

wherein said first and third thin film transistors are n-channel transistors and said second thin film transistor is a p-channel transistor.

6. A method of manufacturing a semiconductor device, comprising the steps of:

forming an insulating film on a surface of a substrate, at least a partial area of the surface exposing a semiconductor region;

forming a conductive film on the insulating film;

covering a partial upper surface of the conductive film with a resist pattern;

etching the conductive film by using the resist pattern as a mask, said etching step being executed under conditions that reaction byproducts during etching being attached on side walls of the patterned conductive film;

etching the insulating film by using as a mask the patterned conductive film and side wall additive attached to the side walls of the conductive film;

removing the side wall additive; and

implanting impurities in the semiconductor region of the substrate under conditions that the impurities transmit through the insulating film exposed under the removed side wall additive.

7. A method of manufacturing a semiconductor device according to claim 6, wherein the substrate includes an insulating underlie substrate and a semiconductor film formed on the underlie substrate.

8. A method of manufacturing a semiconductor device according to claim 6, wherein said conductive film etching step is executed in such a manner that the

substrate is placed in a chamber of a two-frequency plasma etching system, with the conductive film being directed upward and a power supplied to a high frequency power supply means disposed above the substrate is set larger than a power supplied to another high frequency power supply means disposed under the substrate.

9. A method of manufacturing a semiconductor device according to claim 6, wherein said insulating film etching step is executed in such a manner that the substrate is placed in a chamber of a two-frequency plasma etching system, with the insulating film being directed upward and a power supplied to a high frequency power supply means disposed under the substrate is set larger than a power supplied to another high frequency power supply means disposed above the substrate.